REMARKS

I. Introduction

Claims 80-82, 85, and 87-90 are pending in the above application.

Claims 80-82, 85, and 87-90 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by Killian et al. (U.S. Pat No. 5,420,992), and also stand simultaneously rejected under 35 U.S.C. §102(b) as allegedly anticipated by Boutaud et al. (U.S. Pat. No. 5,072,418).

II. Amendments

Claims 1-79 were previously canceled, and claims 83, 84, 86, and 91-94 are canceled by this Amendment.

Claims 1-79, 83, 84, 86, and 91-94 have been canceled without prejudice or disclaimer. Applicant reserves the right to file a divisional application on canceled claims.

Claims 80, 85, 87, and 88 are currently amended in an effort to clarify the intended subject matter of the present invention. The amendments to the claims have been made with respect to the original patent claims as set forth by MPEP 1453.

No new matter has been added.

III. Prior Art Rejections

A. Killian et al. (U.S. Pat No. 5,420,992)

Claims 80-82, 85, and 87-90 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Killian et al. (U.S. Pat. No. 5,420,992) (hereafter "Killian").

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference as arranged in the claim. See, *Akzo N.V. v. U.S. Int'l Trade*

Commission, 808 F.2d 1471 (Fed. Cir. 1986); *Connell v. Sears, Roebuck & Co.*, 220 USPQ 193, 198 (Fed. Cir. 1983).

Killian does not disclose all of the elements of independent claim 80. Killian does not disclose a "processor for operating on certain data in accordance with an instruction in a program, said instruction designating at least one of a first register and a second register, said processor comprising: a first unit configured to perform sign-extending of the certain data if the instruction designates the second register; a second unit configured to perform zero-extending of the certain data if the instruction designates the first register."

Killian, column 8, lines 21-25, merely discloses "In the case of shift instructions, the contents of one source register are shifted by a specified number or by a number defined by the low order bits of the content of a source register, sign-extended or zero-extended, and stored in the destination register." Killian does not, however, disclose a processor for operating on the certain data in different manners (i.e., sign-extending or zero-extending) in accordance with "an instruction designating at least one of a first register and a second register."

Similarly, Killian does not disclose all of the elements of independent claims 85 and 88, which similarly require operating on the certain data in different manners (i.e., sign-extending or zero-extending) depending upon the register designated by the instruction.

Thus, all of the claim limitations of independent claim 80, 85, and 88 are not disclosed by the prior art, and therefore the independent claims are not anticipated by Killian.

Accordingly, as independent claims 80, 85, and 88 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon (82, 87, and 89-90 respectively) are also patentable. In addition, it is respectfully submitted that the dependent

claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

B. Boutaud et al. (U.S. Pat. No. 5,072,418)

Claims 80-82, 85, and 87-90 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Boutaud et al. (U.S. Pat. No. 5,072,418) (hereafter "Boutard").

As noted, anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference as arranged in the claim. See, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986); *Connell v. Sears, Roebuck & Co.*, 220 USPQ 193, 198 (Fed. Cir. 1983).

Boutaud merely discloses "[a] processor scaling shifter 65 has a 16-bit input connected to a data bus 111D via a multiplexer (MUX) 73, and a 32-bit output connected to the ALU 21 via a multiplexer 77. The scaling shifter 65 produces a left-shift of [sic] to 16 bits on the input data, as programmed by instruction or defined in a shift count register (TREGl) 81. The LSBs (least significant bits) of the output are filled with zeros, and the MSBs (most significant bits) may be either filled with zeros or sign-extended, depending upon the state of the sign-extension mode bit SXM of the status register STl in a set of registers 85 of FIG. 1B. Additional shift capabilities enable the processor 11 to perform numerical scaling, bit extraction, extended arithmetic, and overflow prevention" at column 5, line 64, to column 6, line 9.

Boutaud further discloses "Scaling shifter 65 advantageously has a 16-bit input connected to the data bus lllD via MUX 73 and a 32-bit output connected to the ALU 21 via MUX 77. The scaling shifter prescaler 65 produces a left shift of 0 to 16 bits on the input data, as programmed by loading a COUNT register 199. The shift count is specified by a constant embedded in the

instruction word, or by a value in register TREGl. The LSBs of the output of prescaler 65 are filled with zeros, and the MSBs may be either filled with zeros or sign-extended, depending upon the status programmed into the SXM (sign-extension mode) bit of status register STl" at column 15, lines 3-14.

Importantly, Boutaud does not disclose a processor for operating on certain data in accordance with "an instruction designating at least one of a first register and a second register." In other words, Boutaud does not disclose a processor for operating on certain data in different manners depending upon the register designated by the instruction.

Similarly, Boutaud does not disclose all of the elements of independent claims 85 and 88, which similarly require operating on certain data in different manners depending upon the register designated by the instruction.

Thus, all of the claim limitations of independent claim 80, 85, and 88 are not disclosed by the prior art, and therefore the independent claims are not anticipated by Boutaud.

Accordingly, as independent claims 80, 85, and 88 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon (82, 87, and 89-90 respectively) are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

IV. Conclusion

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's

amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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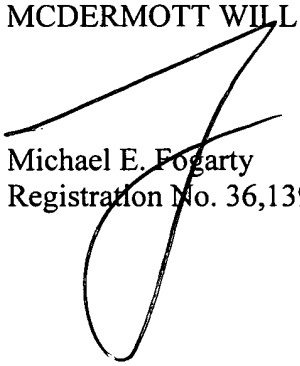

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